

Appl. No. 10/605,499
Amdt. dated January 24, 2006
Reply to Office action of November 02, 2005

Amendments to the Specification:

Please replace paragraph [0002] with the following amended paragraph:

[0002] The present invention relates to a method of fabricating a low temperature polysilicon thin film transistor liquid crystal display (LTPS TFT-LCD), and more particularly, to a method of fabricating a LTPS TFT-LCD composed of P-type LTPS TFT by utilizing seven ~~photo-etching-processes~~ photo-etching processes (PEPs).

Please replace paragraph [0006] with the following amended paragraph:

[0006] As shown in Fig.1, an amorphous -silicon (α -Si)- thin film (not shown) is first formed on the surface of the insulation substrate 10. Then, an excimer laser annealing (ELA) process is performed to re-crystallize the amorphous silicon thin film into a polysilicon layer (not shown). A first ~~photo-etching-processes~~ photo-etching processes (PEP-1) is thereafter performed to define an active area 12 in the pixel array area 11 and at least one active area 14 in the periphery circuit area 13. A source region (not shown), a drain region (not shown), a channel region (not shown), and a predetermined region for a bottom storage electrode (not shown) are formed in the active area 12; a source region (not shown), a drain region (not shown), and a channel region (not shown) are formed in each active area 14.

Please replace paragraph [0007] with the following amended paragraph:

[0007] As shown in Fig.2, a second ~~photo-etching-processes~~ photo-etching process (PEP-2) is performed to form a photoresist layer 16 on the top surface of the insulation substrate 10. The photoresist layer 16 is used to define the location for the bottom storage electrode 18 in the pixel array area 11. After that, an ion implantation process is performed to add high concentration N-type dopants into the exposed portion of the active area 12 in the pixel array area 11, completing the fabrication of the bottom storage electrode 18.

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Please replace paragraph [0008] with the following amended paragraph:

5 [0008] The photoresist layer 16 is removed. As shown in Fig.3, an isolation layer 22 and a first conductive layer (not shown) are formed on a surface of the entire structure sequentially. Then a third ~~photo-etching-processes~~ photo-etching process (PEP-3) is performed to simultaneously form a gate electrode 24 of a TFT, a top storage electrode 26 on the bottom storage electrode 18 in the pixel array area 11, a gate electrode 28 of an NMOS and a gate electrode 32 of a PMOS in the periphery circuit area 13.

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Please replace paragraph [0011] with the following amended paragraph:

15 [0011] As shown in Fig.5, a fourth ~~photo-etching-processes~~ photo-etching process (PEP-4) is performed to form a photoresist layer 54 on a surface of the entire structure. The photoresist layer 54 covers the gate electrode 24 and the predetermined region for a lightly doped drain 56 in the pixel array area 11 and simultaneously covers the predetermined region for a PMOS in the periphery circuit area 13. An ion implantation process is thereafter performed to dope high concentration N-type ions to form a source electrode 62 and a drain electrode 64 of a TFT 58 in the active area 12 in the pixel array area 11 and simultaneously form a source electrode 68 and a drain electrode 72 of an NMOS 66 in the active area 14 in the periphery circuit area 13.

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Please replace paragraph [0012] with the following amended paragraph:

25 [0012] The photoresist layer 54 is removed. As shown in Fig.6, a fifth ~~photo-etching-processes~~ photo-etching process (PEP-5) is performed to form a photoresist layer 74 on a surface of the entire structure. The photoresist layer 74 exposes the predetermined region for the PMOS 76 in the periphery circuit area 13. After that, an

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ion implantation process is performed to dope high concentration P-type ions to form a source electrode 78 and a drain electrode 82 of the PMOS 76 in the active area 14 in the periphery circuit area 13. Due to the high concentration P-type ions implanted in this ion implantation process, the previously formed N-type lightly doped drain 52 (shown in Fig.5) is compensated and the source electrode 78 and the drain electrode 82 are thus formed.

Please replace paragraph [0013] with the following amended paragraph:

[0013] The photoresist layer 74 is then removed. As shown in Fig.7, an isolation layer 84 is formed on a surface of the entire structure. The isolation layer 84 covers the gate electrodes 24, 28, 32 and the top storage electrode 26. Then a sixth ~~photo-etching-processes~~ photo-etching process (PEP-6) is performed to remove portions of the isolation layer 84 to form a plurality of contact holes 85. The contact holes 85 are electrically connected to the source electrodes 62, 68, 78 and the drain electrodes 72, 82, respectively. A source wire 86, electrically connected to the source electrode 62, is formed on top of the isolation layer 84 in the pixel array area 11. Source wires 88, electrically connected to the source electrodes 68, 78 respectively, are formed on top of the isolation layer 84 in the periphery circuit area 13. A wire 92 electrically connecting the NMOS 66 to the PMOS 76 is formed to complete the manufacturing of the CMOS.

Please replace paragraph [0014] with the following amended paragraph:

[0014] As shown in Fig.8, an isolation layer 94 is formed on a surface of the entire structure to cover the isolation layer 84, the source wires 86, 88, and the wire 92. A seventh ~~photo-etching-processes~~ photo-etching process (PEP-7) is performed to remove portions of the isolation layer 94 to form a contact hole 95. The contact hole 95 extends downward and is electrically connected to the drain electrode 64. A transparent

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conductive layer is thereafter formed on the isolation layer 94. Finally, an eighth photo-etching process (PEP-8) is performed to remove portions of the transparent conductive layer to form a pixel electrode 96 on the isolation layer 94. The pixel electrode 96 is electrically connected to the drain electrode 64 downward through the contact hole 95 filled with the transparent conductive layer (not shown) to complete the fabrication of the LTPS TFT-LCD 98.

Please replace paragraph [0017] with the following amended paragraph:

[0017] It is therefore an object of the claimed invention to provide a method of fabricating a LTPS TFT-LCD; specifically, a method of fabricating a LTPS TFT-LCD composed of P-type LTPS TFTs with precise alignment and superior reliability by utilizing seven ~~photo-etching processes~~ photo-etching processes.

Please replace paragraph [0018] with the following amended paragraph:

[0018] According to the claimed invention, an insulation substrate is provided first. At least one active area of a P-type LTPS TFT and at least one bottom storage electrode of a storage capacitor, composed of polysilicon, are formed on a surface of the insulation substrate. Each active area comprises a source region, a drain region, and a channel region. Then a second ~~photo-etching processes~~ photo-etching process and a P-type ion implantation process are performed to form at least one source electrode and at least one drain electrode in each source region and each drain region, respectively, and to simultaneously dope dopants into each bottom storage electrode. A metal layer is thereafter formed on the insulation substrate to cover each active area and each bottom storage electrode. After that, a third ~~photo-etching processes~~ photo-etching process is performed to remove portions of the metal layer to form a gate electrode of each P-type low temperature polysilicon thin film transistor on each channel region to complete the

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fabrication of each P-type LTPS TFT, and to form a top storage electrode of each storage capacitor on each bottom storage electrode to complete the fabrication of each storage capacitor.

- 5 Please replace paragraph [0019] with the following amended paragraph:

[0019] A first isolation layer is then formed on the insulation substrate to cover each gate electrode and each top storage electrode. A fourth ~~photo-etching-processes~~ photo-etching process is thereafter performed to remove portions of the first isolation layer to form at least one first contact hole electrically connected to each source electrode, each drain electrode, and each gate electrode. After that, a conductive layer is formed on the first isolation layer to fill in each first contact hole. A fifth ~~photo-etching-processes~~ photo-etching process is then performed to remove portions of the conductive layer to form at least one source wire and at least one drain wire on the first isolation layer. Each source wire and each drain wire are electrically connected to each source electrode and each drain electrode through each first contact hole respectively. Finally, a second isolation layer is formed on the insulation substrate to cover the first isolation layer, each source wire, and each drain wire.

- 20 Please replace paragraph [0020] with the following amended paragraph:

[0020] Since the claimed invention method fabricates the LCD composed of P-type LTPS TFTs by utilizing five ~~photo-etching-processes~~ photo-etching process, not only is the number of the photolithography processes and ion implantation processes decreased to simplify the process, the risk of alignment errors occurring is also reduced to improve the device defect problem. As a result, high reliability performance is improved. Furthermore, since the leakage current of the P-type LTPS TFT is lower than that of the N-type LTPS TFT, and the leakage current of the P-type LTPS TFT is more easily controlled, the

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present invention method effectively improves the electrical performance of the display, and significantly improves the image quality.

Please replace paragraph [0026] with the following amended paragraph:

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[0026] The present invention method first utilizes a sputtering process or other deposition process to form an amorphous silicon thin film (not shown) on the surface of the insulation substrate 100. Then, an excimer laser annealing (ELA) process is performed to re-crystallize the amorphous silicon thin film into a polysilicon layer (not shown). A first
10 ~~photo-etching processes~~ photo-etching process is thereafter performed to remove portions of the polysilicon layer to form an active area 102 in the pixel array area 101 and at least one active area 104 in the periphery circuit area 103. A source region (not shown), a drain region (not shown), a channel region (not shown), and a predetermined region for a
15 bottom storage electrode (not shown) are comprised on a surface of the active area 102. A source region (not shown), a drain region (not shown), and a channel region (not shown) are comprised on a surface of each active area 104. It should be noted that the excimer laser annealing process might be performed after the first ~~photo-etching processes~~
photo-etching process.

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Please replace paragraph [0027] with the following amended paragraph:

[0027] As shown in Fig.10, a second ~~photo-etching processes~~ photo-etching process is performed to form a first mask 106 on the insulation substrate 100. The first mask 106 exposes the source region 105, the drain region 107, and the bottom storage electrode 108
25 in the active area 102 in the pixel array area 101, and simultaneously exposes the source regions 109 and the drain regions 111 in the active area 104 in the periphery circuit area 103. In order to integrate the devices, the bottom storage electrode 108 is contiguous to the drain region 107 in the preferred embodiment of the present invention. An ion

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implantation process is thereafter performed to dope high concentration P-type ions by utilizing the first mask 106 as a mask. A source electrode 112 and a drain electrode 114 are formed in the active area 102 in the pixel array area 101, the bottom storage electrode 108 is doped with P-type dopants, and source electrodes 116 and drain electrodes 118 are simultaneously formed in the active area 104 in the periphery circuit area 103.

Please replace paragraph [0028] with the following amended paragraph:

[0028] The first mask 106 is removed after the ion implantation process. As shown in Fig.11, a first isolation layer (not shown) and a metal layer (not shown) are formed on a surface of the entire structure sequentially. The first isolation layer and the metal layer cover the active areas 102, 104, and the bottom storage electrode 108. The first isolation layer is a single-layered structure or a doublelayered structure. The material composition of the first isolation layer comprises ~~silicon oxide deposited by utilizing tetra-ethyl-ortho-silicate (TEOS) as a reaction gas, silicon nitride, etc.~~ silicon oxide, silicon nitride, or silicon oxide which is deposited by utilizing tetra-ethyl-ortho-silicate as a reaction gas, etc. The material composition of the metal layer comprises tungsten (W) or chrome (Cr). Furthermore, a cleaning process may be performed before forming the first isolation layer. By utilizing an ozone solution, the surfaces of the active areas 102, 104 and a surface of the bottom storage electrode 108 are cleaned to remove the native oxide layer (not shown) on the active areas 102, 104 and the bottom storage electrode 108. The surfaces of the active areas 102, 104 and the bottom storage electrode 108 thus become passive to prevent the polysilicon from oxidizing before the first isolation layer is formed to ensure the channel region is not contaminated.

Please replace paragraph [0029] with the following amended paragraph:

[0029] A third ~~photo-etching processes~~ photo-etching process is thereafter performed to

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remove portions of the first isolation layer and the metal layer to form a gate insulating layer 124 and a gate electrode 126 on the channel region 123 in the pixel array area 101 and complete the fabrication of the P-type LTPS TFT 128, and to form a capacitor dielectric layer 132 and a top storage electrode 134 on top of the bottom storage electrode 108 and complete the fabrication of the storage capacitor 136. Simultaneously, gate insulating layers 138, 144 and gate electrodes 142, 146 of the P-type LTPS TFT are formed on the channel region 137 in the periphery circuit area 103 to complete the fabrication of the P-type LTPS TFT 148A, 148B.

10 Please replace paragraph [0030] with the following amended paragraph:

[0030] It should be noted that since the first isolation layer, being a single-layered structure or a double-layered structure, is not etched up or even not etched at all when performing the third ~~photo-etching-processes~~ photo-etching process. The first isolation layers being underneath the gate electrodes 126, 142, 146 and the top storage electrode 134 are taken as the gate insulating layers 124, 138, 144 and the capacitor dielectric layer 132. In the figures, the first isolation layer is shown completely removed to illustrate the preferred embodiment of the present invention. In addition, the thicknesses of the gate insulating layers 124, 138, 144 are all less than the thickness of the gate electrodes 126, 142, 146.

Please replace paragraph [0031] with the following amended paragraph:

[0031] As shown in Fig.12, a second isolation layer 152 is formed on a surface of the entire structure to cover the gate electrodes 126, 142, 146 and the top storage electrode 134. The material composition of the second isolation layer 152 comprises silicon oxide, silicon nitride, or silicon oxynitride. After that, a fourth ~~photo-etching-processes~~ photo-etching process is performed to remove portions of the second isolation layer 152

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to form a plurality of first contact holes 154, electrically connected to the source electrodes 112, 116 and the drain electrodes 114, 118, respectively.

Please replace paragraph [0032] with the following amended paragraph:

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[0032] A conductive layer (not shown) is thereafter formed on a surface of the second isolation layer 152. The conductive layer fills up the first contact holes 154. Then a fifth ~~photo-etching-processes~~ photo-etching process is performed to remove portions of the conductive layer to form a source wire 156, electrically connected to the source electrode 10 112, on the surface of the second isolation layer 152 used as a data line of the LTPS TFT-LCD, and to form a drain wire 158, electrically connected to the drain electrode 114, in the pixel array area 101. Source wires 162, electrically connected to the source electrodes 116, and drain wires 164, electrically connected the drain electrodes 118, are formed on the surface of the second isolation layer 152 in the periphery circuit area 103 15 depending on practical requirements. It should be noted that a contact hole and a wire may be formed on top of the gate electrode.

Please replace paragraph [0033] with the following amended paragraph:

20 [0033] As shown in Fig.13, a third isolation layer 166 is formed on a surface of the entire structure to cover the second isolation layer 152, the source wires 156, 162, and the drain wires 158, 164. The material composition of the third isolation layer 166, being a planarization layer, comprises silicon oxide, silicon nitride, or silicon oxide deposited by utilizing tetra-ethyl-ortho-silicate as a reaction gas. A sixth ~~photo-etching-processes~~ 25 photo-etching process is performed to remove portions of the third isolation layer 166 to form a second contact hole 168 electrically connected to the drain wire 158. After that, a transparent conductive layer (not shown) is formed on the third isolation layer 166. The material composition of the transparent conductive layer comprises indium tin oxide

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(ITO) or indium zinc oxide (IZO). Finally, a seventh ~~photo-etching-processes~~
photo-etching process is performed to remove portions of the transparent conductive layer
to form a pixel electrode 172 on the third isolation layer 166. The pixel electrode 172 is
electrically connected to the drain wire 158 and the drain electrode 114 downward through
5 the second contact hole 168 filled with the transparent conductive layer to complete the
fabrication of the low temperature polysilicon thin film transistor liquid crystal display
174.

Please replace paragraph [0035] with the following amended paragraph:

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[0035] The present invention method first utilizes a sputtering process or other deposition
process to form an amorphous silicon thin film (not shown) on the surface of the
insulation substrate 200. Then, an excimer laser annealing (ELA) process is performed to
re-crystallize the amorphous silicon thin film into a polysilicon layer (not shown). A first
15 ~~photo-etching-processes~~ photo-etching process is thereafter performed to remove portions
of the polysilicon layer to form an active area 202 in the pixel array area 201 and at least
one active area 204 in the periphery circuit area 203. A source region (not shown), a drain
region (not shown), a channel region (not shown), and a predetermined region for a
bottom storage electrode (not shown) are formed on a surface of the active area 202. A
20 source region (not shown), a drain region (not shown), and a channel region (not shown)
are formed on a surface of each active area 204. It should be noted that the excimer laser
annealing process ~~[[may]]~~ might be performed after the first ~~photo-etching-processes~~
photo-etching process.

25 Please replace paragraph [0036] with the following amended paragraph:

[0036] As shown in Fig.15, a first isolation layer 206 is formed on a surface of the
insulation substrate 200. The first isolation layer 206 covers the active areas 202, 204.

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The first isolation layer 206 is a single-layered structure or a double-layered structure. The material composition of the first isolation layer 206 comprises ~~silicon oxide deposited by utilizing tetra-ethyl-ortho-silicate (TEOS) as a reaction gas, silicon oxide, or silicon nitride.~~ silicon oxide, silicon nitride, or silicon oxide which is deposited by utilizing tetra-ethyl-ortho-silicate as a reaction gas. Furthermore, a cleaning process may be performed before forming the first isolation layer 206. By utilizing an ozone solution, the surfaces of the active areas 202, 204 are cleaned to remove the native oxide layer (not shown) on the active areas 202, 204. The surfaces of the active areas 202, 204 thus become passive to prevent the polysilicon from oxidizing before the first isolation layer 206 is formed to ensure the channel region (not shown) is not contaminated.

Please replace paragraph [0037] with the following amended paragraph:

[0037] Then, a second ~~photo-etching-processes~~ photo-etching process is performed to form a first mask 208 on the insulation substrate 200. The first mask 208 exposes the source region 205, the drain region 207, and the bottom storage electrode 210 in the active area 202 in the pixel array area 201, and simultaneously exposes the source regions 209 and the drain regions 211 in the active area 204 in the periphery circuit area 203. In order to integrate the devices, the bottom storage electrode 210 is contiguous to the drain region 207 in the preferred embodiment of the present invention. An ion implantation process is thereafter performed to dope high concentration P-type ions by utilizing the first mask 208 as a mask. A source electrode 212 and a drain electrode 214 of a P-type LTPS TFT (not shown) are formed in the active area 202 in the pixel array area 201, the bottom storage electrode 210 is doped with P-type dopants, and source electrodes 216 and drain electrodes 218 of P-type LTPS TFTs (not shown) are simultaneously formed in the active area 204 in the periphery circuit area 203.

Please replace paragraph [0038] with the following amended paragraph:

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[0038] The first mask 208 is removed after the ion implantation process. As shown in Fig.16, a metal layer (not shown) is formed on the surface of insulation substrate 200. The metal layer covers the first isolation layer 206, the active areas 202, 204, and the bottom storage electrode 210. The material composition of the metal layer comprises tungsten (W) or chrome (Cr). As shown in Fig.17, a third ~~photo-etching-processes~~ photo-etching process is thereafter performed to remove portions of the first isolation layer 206 and the metal layer to form a gate insulating layer 224 and a gate electrode 226 on the channel region 223 in the pixel array area 201 and complete the fabrication of the P-type LTPS TFT 228, and to form a capacitor dielectric layer 232 and a top storage electrode 234 on top of the bottom storage electrode 210 and complete the fabrication of the storage capacitor 236. Simultaneously, gate insulating layers 238, 244 and gate electrodes 242, 246 are formed on the channel regions 237 in the periphery circuit area 203 to complete the fabrication of the P-type LTPS TFTs 248A, 248B.

Please replace paragraph [0039] with the following amended paragraph:

[0039] It should be noted that since the first isolation layer 206, being a single-layered structure or a double-layered structure, is not etched up or even not etched at all when performing the third ~~photo-etching-processes~~ photo-etching process. The first isolation layers 206 being underneath the gate electrodes 226, 242, 246 and the top storage electrode 234 are taken as the gate insulating layers 224, 238, 244 and the capacitor dielectric layer 232. In the figures, the first isolation layer 206 is shown completely removed to illustrate the preferred embodiment of the present invention. In addition, the thicknesses of the gate insulating layers are all less than the thickness of the gate electrodes.

Please replace paragraph [0040] with the following amended paragraph:

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[0040] As shown in Fig.18, a second isolation layer 252 is formed on a surface of the entire structure to cover the gate electrodes 226, 242, 246 and the top storage electrode 234. The material composition of the second isolation layer 252 comprises silicon oxide, silicon nitride, or silicon oxynitride. After that, a fourth ~~photo-etching-processes~~ photo-etching process is performed to remove portions of the second isolation layer 252 to form a plurality of first contact holes 254, electrically connected to the source electrodes 212, 216 and the drain electrodes 214, 218, respectively.

10 Please replace paragraph [0041] with the following amended paragraph:

[0041] A conductive layer (not shown) is thereafter formed on a surface of the second isolation layer 252. The conductive layer fills up the first contact holes 254. Then a fifth ~~photo-etching-processes~~ photo-etching process is performed to remove portions of the conductive layer to form a source wire 256, electrically connected to the source electrode 212, on the surface of the second isolation layer 252 used as a data line of the LTPS TFT-LCD, and to form a drain wire 258, electrically connected to the drain electrode 214 in the pixel array area 201. Source wires 262, electrically connected to the source electrodes 216, and drain wires 264, electrically connected the drain electrodes 218, are formed on the surface of the second isolation layer 252 in the periphery circuit area 203 depending on practical requirements. It should be noted that a contact hole and a wire ~~[[may]]~~ might be formed on top of the gate electrode.

Please replace paragraph [0042] with the following amended paragraph:

[0042] As shown in Fig.19, a third isolation layer 266 is formed on a surface of the entire structure to cover the second isolation layer 252, the source wires 256, 262, and the drain wires 258, 264. The third isolation layer 266, being a planarization layer, comprises a

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silicon oxide layer, a silicon nitride layer, or a silicon oxide layer deposited by utilizing tetra-ethyl-ortho-silicate (TEOS) as a reaction gas. A sixth ~~photo-etching-processes~~ photo-etching process is performed to remove portions of the third isolation layer 266 to form a second contact hole 268 electrically connected to the drain wire 258. After that, a
5 transparent conductive layer (not shown) is formed on a surface of the third isolation layer 266. The material composition of the transparent conductive layer comprises indium tin oxide (ITO) or indium zinc oxide (IZO). Finally, a seventh ~~photo-etching-processes~~ photo-etching process is performed to remove portions of the transparent conductive layer to form a pixel electrode 272 on the third isolation layer 266. The pixel electrode 272 is
10 electrically connected to the drain wire 258 and the drain electrode 214 downward through the second contact hole 268 filled with the transparent conductive layer to complete the fabrication of the LTPS TFT-LCD 274.

Please replace paragraph [0044] with the following amended paragraph:

15 [0044] In comparison with the prior art method of fabricating the LTPS TFT-LCD, the present invention discloses a method of fabricating a LCD composed of P-type LTPS TFTs by utilizing seven ~~photo-etching-processes~~ photo-etching process. The number of photolithography processes and ion implantation processes is decreased to simplify the
20 process. The risk of alignment errors is also reduced to improve the device defect problem to improve the high reliability performance. Furthermore, since the leakage current of the P-type LTPS TFT is lower than that of the N-type LTPS TFT, and the leakage current of the P-type LTPS TFT is more easily controlled, the present invention effectively improves
25 the electrical performance and image quality of a LCD.